IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Koichi HANAFUSA et al.

Application No.:

NEW APPLICATION

Filed:

July 22, 2003

For:

AMPLIFIER CIRCUIT AND POWER SUPPLY PROVIDED

THEREWITH

INFORMATION DISCLOSURE STATEMENT (SUBMISSION CONCURRENT WITH THE FILING OF A NEW PATENT APPLICATION)

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 July 22, 2003

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on PTO-1449, attached hereto.

II. <u>COPIES</u>

\boxtimes	Submitted herewith is a legible copy of (i) each U.S. and foreign patent; (ii) each
	publication or that portion which caused it to be listed; and (iii) all other information
	or that portion which caused it to be listed.

This application is a National Phase of a PCT application. Some or all of the
documents listed on the PTO-1449 are not enclosed because they were cited in the
International Search Report and copies should be forwarded from the International
Search Authority. If copies are needed, please contact the undersigned.

III,			KPLANATION OF THE RELEVANCE (a) t one box)						
	a.		DOCUMENTS IN THE ENGLISH LANGUAGE						
			The attached patents, publications, or other information in the English language do not require a statement of relevancy.						
	b.		DOCUMENTS NOT IN THE ENGLISH LANGUAGE						
	•		A concise explanation of the relevance of all patents, publications, of other information listed that is not in the English language is a follows:						
		.							
	c.	\bowtie	OTHER						

For the Examiner's convenience, we attach hereto U.S. Patent No. 5,859,757, which is the corresponding U.S. equivalent of Japanese Publication for Unexamined Patent Application No. 111722/1998. Submission of the English language equivalent(s) is deemed to satisfy the requirement for a concise explanation of relevancy.

For the article "Designing of Practical Analog Electronic Circuits", see attached statement of relevancy and partial English translation enclosed herewith.

FEES

This Information Disclosure Statement is being filed concurrently with the filing of a new patent application; therefore, no fee is required.

If The Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 08-0750.

New U.S. Application Docket No. 12480-00017/US

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, P.L.C

By: _

Donald J. Daley, Reg. No. 34,313

P.O. Box 8910

Reston, Virginia 20195

(703) 668-8000

DJD:me

Enclosures: Form PTO-1449(s)

Documents

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Form PTO	-1449	ATTY DOCKET NO. 12480-000017/US	APPLICATION NO. NEW APPLICATION					
	INFORMATION DISCLOSURE CI IN AN APPLICATION	APPLICANT Koichi HANAFUSA, Takao KANZAKI		CONF. NO. Unknown GROUP Unknown				
	(Use several sheets if necessary	FILING DATE July 22, 2003						
		U.S. PATENT DO	CUMENTS		2, "			
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS		DATE OPRIATE	
	5,859,757	1/12/1999	Hanafusa et al.					
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	OCUMENTS (Include Name of the author (in al, symposium, catalog, etc.) date, page(s), volu					(book, ma	igazine,	
	KAZUO WATANABE, "De 22, 1996, pages 109 – 112.	KAZUO WATANABE, "Designing of Practical Analog Electronic Circuits", Sougou-Denshi Shuppansha, June 22, 1996, pages 109 – 112.						
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